Remarks

In the Office Action mailed on 24 July 2007, the Examiner rejected claims 1-6, 8, 9, 11, 12, 15, 16, 18, and 19 under 35 U.S.C. §102(e) as anticipated by Mullendore (United States Patent Publication number 2003/0185154). The Examiner also rejected claims 7, 10, 13, 17, 21, and 22 under 35 U.S.C. §103(a) as unpatentable over Mullendore in view of Liu (United States Patent Publication Number 2004/0117441) and rejected claims 14 and 20 under 35 U.S.C. §103(a) as unpatentable over Mullendore in view of well-known art.

Applicant traverses the rejections and requests reconsideration and withdrawal thereof. Applicant has amended independent claims 1, 11, 15, and 18 for editorial clarity and to better protect the invention. Claims 8, 9, 12, 14, 16, 19, and 20 have been cancelled with their essential recitations integrated into respective base claims.

35 U.S.C. §§ 102 and 103 Rejections

The Examiner rejected all claims (1-22) under 35 U.S.C. §102 as anticipated by Mullendore or under §103 as unpatentable over Mullendore in view of Liu or "well known art". Applicant traverses the rejections.

As regards independent claim 1, the Examiner points to paragraph 0072 in describing figure 7 of Mullendore as teaching all recited elements. While Applicant admits that Mullendore uses the word "cache" he provides no explanation of its function other than as a buffer to hold data in far-end switch 240 until an addressed far-end target device 245 is ready to accept more data. In other words, Mullendore teaches nothing more than a simple buffer for "speed matching" in the transfers between an initiator 235 and a target 245. Nothing in Mullendore teaches the complexity of a router that processes the block level storage requests exchanged between a first and second iSCSI device coupled through the router. By so processing the block level storage requests, the router of claim 1 may store data blocks in its local cache memory as they are exchanged between the first and second devices. In addition, when the first device issues a read block level storage request, the router may complete the request by returning data blocks from its local cache memory without ever forwarding the storage request to the second device (e.g., without forwarding a read request to the target device.).

In hopes of advancing prosecution of this application, Applicant has amended claim 1 to clearly recite the intended purpose of the cache memory within the claimed apparatus. Specifically, claim 1 includes recitations that the cache memory is used to store data blocks exchanged between a first and second device coupled to the router and further recites that the router may complete a read block level storage request by return of requested data directly from its cache memory without forwarding the request to the second device. Such a caching feature in a TCP/IP router is simply not taught or reasonably suggested by the Mullendore or any art of record, considered individually or in any combination.

Independent claims 11, 15, and 18 were rejected similarly as anticipated by Mullendore and have been similarly amended to clarify the intended operation of a cache memory in the router (as distinct from a mere buffer used for speed matching purposes as taught by Mullendore).

Dependent claim 14 (dependent from 11) and 20 (dependent from 18) included similar recitations and were rejected by the Examiner under §103 as unpatentable over Mullendore in view of "well-known" prior art. Applicant strongly disagrees. There is no art provided by the Examiner or any suggestion in the art to apply cache memory management techniques and structures within a network appliance router (a TCP/IP router). As noted, Mullendore suggest nothing more than well-known speed-matching buffering. Though he misuses the word "cache" in reference to his buffer he makes clear that the buffer is used merely to hold data (in far-end switch 240) until the receiving device (target 245) is ready to receive more data - the very essence of a speed-matching buffer. Mullendore suggests nothing more of use of the buffer for cache purposes such as recited in claims 14 and 20 (or other claims now cancelled). These caching features in a network appliance router (e.g., a TCP/IP router) are the very essence of the present invention. Thus it is only through improper hindsight applying the teachings of the subject application that the Examiner asserts this "well-known" knowledge.

Claims 8, 9, 12, 14, 16, 19, and 20 included versions of these caching features and are cancelled with their essential recitation added to their respective base claims (1, 11, 15, and 18).

Remaining dependent claims 2-7, 10, 13, 17, 18, 21, and 22 recite additional limitations and thus are maintained to be allowable for at least the same reasons as above and also as dependent from allowable base claims.

Claim 22 was amended to correct a dependency on a now cancelled claim.

In view of the above discussion and the various amendments, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections under §102 and §103.

Conclusion

Applicant has amended independent claims 1, 11, 15, 18, and 22 for editorial clarity to better protect the invention. Applicant has cancelled dependent claims 8, 9, 12, 14, 16, 19, and 20 with their essential recitation integrated into respective base claims. Applicant has traversed and thoroughly discussed the Examiner's rejections of all claims. Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and objections.

Applicant believes that no other fees are due in this matter. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

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